Amendments to the Claims:

This listing of the claims replaces all prior versions, and listings, of the claims in the application.

Listing of Claims:

1.(Currently amended) An automated computer-implemented method for reducing the number of distinct integrated circuit (IC) logic cells used to implement an IC design, said method comprising the steps of:

receiving a functional description for a cell;

receiving a design constraint for said cell, said design constraint related to a context-of-use for said cell in said IC design; and

determining an implementation of said cell based on said functional description and said design constraint, wherein the number of distinct IC logic cells for implementing said IC design is reduced.

2.(Original) The method of claim 1, wherein said constraint is selected from a group of metrics consisting of: timing, power, area, noise margins, slew, input/output capacitances, switching capacitances, drive strength, footprint size, and pin-placement for said cell.

3.(Original) The method of claim 1, further comprising the step of determining whether said functional description and said constraint can be matched by an existing cell.

4.(Original) The method of claim 3, further comprising the step of determining a signature for said cell based on said functional description and said constraint.

5.(Original) The method of claim 4, further comprising the step of evaluating said signature against a signature of an existing cell to determine a possible match.

6.(Currently amended) The method of claim 1, wherein said step of determining comprises at least determining an implementation of one possible input permutation for said cell.

7.(Currently amended) The method of claim 1, wherein said step of determining comprises at least determining an implementation of one possible input complement for said cell.

8.(Currently amended) The method of claim 4, wherein said signature is determined for utilizing ~~each~~ said constraint.

9.(Original) The method of claim 4, wherein said signature comprises a constraint for timing of said cell.

10.(Original) The method of claim 9, wherein said constraint for timing of said cell comprises a sorted list of rise times and fall times.

11.(Original) The method of claim 10, further comprising the step of comparing said sorted set of rise and fall times against a sorted set of available rise and fall times of a cell available in a library, or of a cell created on-the-fly.

12.(Original) The method of claim 1, further comprising the step of characterizing said cell based on said constraint, wherein said constraint is related to a context-of-use for said cell in said IC design.

13.(Currently amended) The method of claim 12, wherein said context-

of-use includes at least a region of said IC design .

14.(Original) The method of claim 12, wherein said context-of-use is utilized to define a set of characterization vectors applicable to said cell.

15.(Currently amended) The method of claim 14, wherein said context-of-use ~~may~~ includes a factor not affecting the size of said set of characterization vectors applicable to said cell.

16. (Original) The method of claim 15, wherein said set of characterization vectors applicable to said cell comprises a set of restrictions on process corners at which said cell is characterized.

17.(Currently amended) The method of claim 12, wherein characterization of said IC design is accomplished by characterizing partitions of said IC design at a transistor level.

18.(Original) The method of claim 17, wherein said partitions are realized as at least one standard-cell.

19.(Currently amended) The method of claim 17, wherein said partitions ~~can be~~are formed in a region of said IC design based on ~~a~~ design criteria.

20.(Currently amended) The method of claim 17, wherein said design criteria ~~is~~ are selected from a group consisting of timing, area, power, and signal integrity.

21.(Original) The method of claim 17, wherein said partitions comply with a standard-cell based IC design flow.

22.(Currently amended) A storage media including computer readable

program instructions for an automated computer-implemented method for reducing the number of distinct integrated circuit (IC) logic cells used to implement an IC design, said storage media comprising:

program instructions for receiving a functional description for a cell;

program instructions for receiving a design constraint for said cell, said design constraint related to a context-of-use for said cell in said IC design; and

program instructions for determining an implementation of said cell based on said functional description and said design constraint, wherein the number of distinct IC logic cells for implementing said IC design is reduced.

Amendment to the Drawings:

The attached sheet of drawings includes changes to Figures 1 and 1a. This sheet replaces the previous version of Figures 1 and 1a. The legend -- PRIOR ART-- has been added to Figures 1 and 1a.

Attachment: Replacement Sheet